REMARKS

The Examiner is thanked for the careful review of this Application. Claims 6, 8, and 26-35 are pending after entry of the present Amendment. Claims 1-5, 7, and 9-25 were cancelled. Claims were amended to better define the invention and to present the rejected claims in better form for consideration on appeal. The amendments do not introduce new matter.

Rejections under 35 U.S.C. § 103(a):

The Office has maintained rejection of claims 6, 8, and 26-35 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,333,255 to Sekiguchi in view of U.S. Patent No. 6,277,728 to Ahn et al. ("Ahn").

It is respectfully submitted that the Office's suggestion that Sekiguchi could be modified in view of Ahn would not have rendered replacing the low-k dielectric material of Sekiguchi with the porous dielectric material of Ahn obvious unless Sekiguchi suggests the desirability of modifying the low-k dielectric material with the porous dielectric material. *In re* Laskowski, 871 F.2d 115, 10 USPQ2d 1297 (CAFC 1989). Thus, the combination of Sekiguchi and Ahn does not raise a *prima facie* case of obviousness against the subject matter defined in amended independent claims 6, 28, and 34 because the suggested combination fails to teach or suggest all of the features defined in independent claims 6, 28, and 34, and if Sekiguchi were to be modified as suggested by the Office, one of ordinary skill in the art would not have arrived at the claimed invention.

At the outset, the Applicants draw the Office's attention to amendments made to independent claims 6, 28, and 34. For instance, independent claim 6 has been amended to specifically recite that the plurality of supporting stubs are not electrically interconnected to the plurality of copper interconnect metallization lines and conductive vias. In the same manner, independent claims 28 and 34 have been amended to recite that the semiconductor device also includes an intermetal dielectric layer as well as a passivation layer formed thereon. Given the amendments to independent claims 6, 28, and 34 and at least the following reasons, the Applicants respectfully request that 103(a) rejection of claims be withdrawn.

It is respectfully submitted that Sekiguchi's multilevel structure implementing gas-dielectric in view of the multilevel interconnect structure having an outer low-K dielectric coating, as shown in Ahn, fails to teach or suggest all of the features of the claimed invention. First, contrary to the Office' assertion, the two inside "lines" as well as the two outside lines (reference number 17) shown in Sekiguchi are wires, and as wires, are configured to enable flow of current between the multiple levels of the semiconductor structure and provide electrical connection. For support, reference is made to Figures 1(a)-9 wherein the two inside lines are in direct contact with the source/drain regions 3 and Sekiguchi, column 18, lines 5-8, wherein Sekiguchi specifically teaches that each insulating film of a given interconnect layer laterally interconnects the wires of the given interconnect layer to each. As such, contrary to the Office' position, the two inside lines provide electrical connections within the structure.

Furthermore, it is respectfully requested that the Office note that Sekiguchi does not teach dividing the wires into two different types with certain wires not being electrically connected to the others. The Applicants respectfully submit that without using the claimed invention as a blue print, the Office would not have been able to arbitrarily divide the wires into two separate types, with each type providing different functions.

Ahn discloses a multilevel interconnect structure that includes an outer low-K dielectric coating. However, Ahn does not teach forming the low-K dielectric coating as an insulating layer around the interconnect metallization lines. Furthermore, in contrast to the teachings of Sekiguchi or Ahn, the supporting stubs of the claimed invention may or may not be formed of the same material as the copper interconnect metallization lines.

Still further, Sekiguchi and Ahn fail to teach forming of an ILD layer and a passivation layer over the substrate surface and the transistor devices, as defined in amended independent claims 28 and 34. In the claimed invention, the material of the ILD layer is a substantially robust material and is used so as to provide ample insulation. In the same manner, the passivation layer is used to protect the active components on the substrate from corrosion and chemical reactions during the fabrication process. Neither Sekiguchi nor Ahn use or suggest using an ILD layer and passivation layer, as defined in independent claims 28 and 34.

Even if the porous low-K dielectric of Ahn were to be used in the multilevel structure of Sekiguchi, one of ordinary skill in the art would not have arrived at the

claimed invention. Specifically, Sekiguchi uses either a carbon insulating layer or silicon dioxide layer and lower and upper silicon dioxide layers as stoppers, or silicon dioxide layer as an insulating layer and silicon nitride lower and upper layers as stoppers. The insulating layers are etched and depending on the embodiment, the multilevel structure is either filled with the gas generated as a result of the oxygen plasma or low-K dielectric constant material. Thus, while the carbon insulating layers or the silicon dioxide layers of the multilevel structure are etched in all of the embodiments of Sekiguchi, all the upper and lower silicon dioxide or silicon nitride layers are remained intact after the etch processes so as to provide and maintain the structural integrity for the multilevel semiconductor device. In short, even if the porous low-K dielectric material of Ahn were to be used in the multilevel structure of Sekiguchi, the modified multilevel structure is not the same as the semiconductor device of the present invention. The modified multilevel structure still includes all the upper and lower silicon dioxide or silicon nitride insulators which in conjunction with the porous low-K dielectric are formed around the interconnect lines, trenches, and vias. As a result, the modified multilevel structure of Sekiguchi would have a higher dielectric constant than the semiconductor of the claimed invention wherein the interconnect metallization lines and conductive vias are isolated by porous dielectric material.

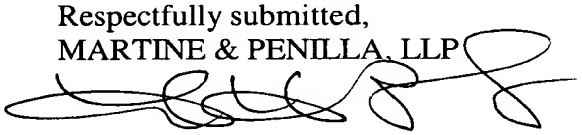
Yet further, neither Sekiguchi nor Ahn teach using a multilevel structure where an ILD layer and passivation layer are formed over the transistor devices (as defined in independent claims 28 and 34) so as to prevent any potential damages to the transistor devices. Thus, if the modified multilevel structure of Sekiguchi were to be modified so as to remove the upper and lower silicon dioxide layers (it must be noted that Sekiguchi neither teaches nor suggest such modification), the removal has to be achieved such that the transistor devices are not damaged. Sekiguchi or Ahn, however, are both silent as to achieving such feature without any damage to the transistor devices. Rather, as described in more detail above, a skilled artisan would not have modified Sekiguchi using Ahn so as to remove the upper and lower silicon dioxide layers or silicon nitride layers, as such modification are against the teachings of Sekiguchi wherein the upper and lower silicon dioxide layers are used to maintain and provide the integrity of the structure.

Accordingly, for at least the above-stated reasons, independent claims 6, 28, and 34, are patentable under 35 U.S.C. § 103(a) over Sekiguchi in view of Ahn. Claims 8, 26, and 27, 29-32, and 35, each of which ultimately depends from the applicable independent claim 6, 28, and 34 are likewise patentable under 35 U.S.C. § 103(a) over Sekiguchi in view of Ahn for at least the same reasons set forth for the applicable independent claim.

The Applicants hereby submits that this Amendment complies with 37 C.F.R. 1.116(b) and should be entered.

In view of the foregoing, the Applicants respectfully submit that all of the pending claims are in condition for allowance. Accordingly, a Notice of Allowance is respectfully requested. If the Examiner has any questions concerning the present Amendment, the Examiner is kindly requested to contact the undersigned at (408) 749-6900, ext. 6913. If any additional fees are due in connection with filing this Amendment, the Commissioner is also authorized to charge Deposit Account No. 50-0805 (Order No. LAM2P246). A duplicate copy of the transmittal is enclosed for this purpose.

Respectfully submitted,
MARTINE & PENILLA, LLP



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